

DAC8831EVM

This user's guide describes the characteristics, operation, and use of the DAC8831EVM – a 16-bit, synchronous-serial-interface, digital-to-analog converter evaluation module (EVM). A complete circuit description, a schematic diagram, and bill of materials are included.

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1 EVM Overview

1.1 Features

- Evaluation board for the 16-bit voltage output DAC8831
- Onboard reference and buffer circuits
- High-speed serial interface
- Modular design for use with a variety of DSP and microcontroller interface boards

1.2 Introduction

The DAC8831 is a single, 16-bit, serial-input, voltage-output, digital-to-analog (DAC) converter operating from a single 3-V to 5-V power supply. This converter provides excellent linearity (1 LSB INL), low glitch, low noise, and fast settling (1 μ S to $\frac{1}{2}$ LSB of full scale output) over the specified temperature range of -40°C to 85°C . The output is unbuffered, which reduces the power consumption and the error introduced by the buffer. An external buffer and DPDT switch are provided on the EVM to allow unipolar and bipolar output operation.

The modular EVM form factor allows direct evaluation of the DAC's performance and operating characteristics. This EVM is compatible with the Texas Instruments 5-6K ([SLAU104](#)), the HPA-MCU

([SLAU106](#)) Interface Boards and additional 3rd party boards such as the HPA449 Demonstration Board from SoftBaugh, Inc. (www.softbaugh.com) and the Speedy33™ from Hyperception, Inc. (www.hyperception.com). Field Programmable Gate Array (FPGA) users may also use the DAC8831EVM in conjunction with a variety of Xilinx FPGA's by obtaining the Texas Instruments Analog Adapter Kit (part number [ADS-TI-AD-DAU](#)) from Avnet Electronics Marketing.

2 Analog Interface

For maximum flexibility, the DAC8831 EVM is designed for easy interfacing to multiple analog sources. [Table 1](#) provides the pinout of connector J1. Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a convenient 10-pin, dual-row header/socket combination at J1. This header/socket provides access to the analog output pins of the DAC through the onboard buffer amplifier. Consult Samtec at www.samtec.com, or call 1-800-SAMTEC-9 for a variety of mating connector options.

Table 1. Pinout of J1

Pin Number	Signal	Description
J1.2	Vout	Buffer voltage output – range depends on the position of SW1 (see section 2.1)
J1.4	Unused	Pins are unused and should be left open for use with future amplifier and sensor output modules.
J1.6	Unused	
J1.8	Unused	
J1.10	Unused	
J1.12	Unused	
J1.14	Unused	
J1.16	Unused	
J1.18	REF(-)	
J1.20	REF(+)	External reference source input (2 V to 5.5 V maximum)
J1.15	Unused	
J1.1–J1.19 (odd)	AGND	Analog ground connections (except J1.15)

2.1 EVM Output Voltage

Switch SW1 provides a means to allow unipolar or bipolar output operation of the DAC8831 EVM. When the slide switch is to the right (screen marked BIP), the output voltage on J1.2 is $\pm V_{REF}$. If the onboard reference is used, this means that the output voltage is -2.5 Vdc to $+2.5$ Vdc. When the switch is to the left (screen marked UNI), the output from the buffer is 0 V to $+2.5$ Vdc.

For a wider dynamic output range, the EVM can be configured to use an external reference by moving the shunt at W1 to cover pins 2-3. In this case, an external reference from $0-V_{DD}$ may be applied to J1.20. For best performance, the external reference must be supplied by a clean dc source.

3 Digital Interface

The DAC8831EVM is designed for easy interfacing to multiple control platforms. [Table 2](#) provides the pinout of connector J2. Samtec part numbers SSW-110-22-F-D-VS-K and TSM-110-01-T-DV-P provide a convenient 10-pin dual row header/socket combination at J2. This header/socket provides access to the digital control and serial data pins of the DAC8831EVM. Consult Samtec at www.samtec.com, or call 1-800-SAMTEC-9 for a variety of mating connector options.

Table 2. Pinout of J2

Pin Number	Signal	Description
J2.1	Unused	
J2.3	SCLK	Serial Clock
J2.5	Unused	
J2.7	\overline{CS}	Chip Select to the DAC. Tied to the Frame Sync for DSP host systems – STE for SPI Host systems
J2.9	Unused	
J2.11	SDI	Serial Data Input
J2.13	Unused	
J2.15	Unused	
J2.17	\overline{LDAC}	Load DAC – Active low signal, enables DAC output updates – jumper configurable (see schematic). When \overline{LDAC} is Low, the DAC latch is simultaneously updated with the content of the input register. Can be controlled by GPIO or tied low via W3.
J2.19	SPARE	

4 Power Supplies

The DAC8831EVM board requires ± 5 Vdc for the analog section. This includes the ground reference operational amplifier (U2) and the output buffer (U1). The +5-V input also supplies the onboard reference (U5) and reference buffer (U4). The output buffer could be configured to run at 0 V to 5 V at the user's option by removing R2 (a 0-ohm resistor) and installing it at location R7 (not installed) found on the underside of the EVM.

Supply voltages of +2.7 Vdc to +5.5 Vdc for the V_{DD} supply to the DAC8831 are also required. When used with one of the previously mentioned interface boards, J3 provides connection to the common power bus described in 5-6K Interface Board User's Guide ([SLAU104](#)).

Table 3 shows the pinout of connector J3.

Table 3. Pinout of J3

Signal	Pin Number		Signal
Unused	1	2	Unused
+5VA	3	4	-5VA
DGND	5	6	AGND
Unused	7	8	Unused
Unused	9	10	+5VD

4.1 Stand-Alone Operation

When used as a stand-alone EVM, the analog power can be applied to J3 pins 3 and 4, referenced to J3 pin 6. Digital power can be applied to J3 pin 10, referenced to J3 pin 5. Optimal performance of the EVM requires a clean, well-regulated power source.

CAUTION

The DAC8831 has a V_{DD} power source requirement of +2.7 Vdc to +5.5 Vdc. If using an external reference source, keep the reference voltage to a level less than or equal to the applied V_{DD} source.

4.2 Reference Voltage

The DAC8831 can be configured to use the onboard reference/buffer circuits (U4 and U5) or an external reference applied to J1.20. Jumper W1 controls the reference source. In the factory default position (shunt on W1 pins 1-2), a 2.5-V reference is supplied by U4. Moving the shunt at W1 to pins 2-3 allows an external reference applied to J1.20 to be used.

Regardless of the reference source, U4 provides a reference buffer to the DAC8831. If no buffer circuit is desired, the EVM user can remove the resistor found at location R5 and apply an external reference directly to TP2, referenced to TP1.

5 EVM Operation

5.1 Analog Output

The analog output is applied directly to J1 (top or bottom side) and can be further applied to optional amplifier and signal conditioning modules. The analog output range depends on the configuration of the EVM and the external reference applied at J1.20 or TP2. See section 3.1 of this user's guide and the DAC8831 data sheet ([SLAS449](#)) to determine the maximum analog output range.

5.2 Digital Control

The digital control signals can be applied directly to J2 (top or bottom side). The DAC8831 EVM can also be connected directly to a DSP or microcontroller interface board such as the 5-6K Interface Board, the HPA-MCU Interface Board or the HPA449. See the DAC8831 product folder on the TI Web site ([www.ti.com](#)) for a current list of compatible interface and/or accessory boards.

5.3 Load DAC (\overline{LDAC})

Jumper W2 is provided to allow the selection of the signals applied to the DAC8831's \overline{LDAC} pin. The factory default condition for the EVM is to place a shunt jumper between pins 1-2 of W3. This ties the \overline{LDAC} pin directly to ground for simultaneous updates of the DAC output buffer. When the shunt is moved to pins 2-3, an external \overline{LDAC} signal may be applied to J2.17 to allow timed updates of the DAC output buffer.

5.4 Default Jumper Locations

Table 4 provides a list of jumpers and switches found on the EVM and their factory default conditions.

Table 4. List of Jumpers and Switches

Jumper	Shunt	Position Jumper Description
W1	Pins 1-2	Controls DAC reference source (default is U5 – 2.5VDC)
W3	Pins 1-2	Controls \overline{LDAC} pin (default is DGND)
SW1	LEFT	Controls analog output voltage (default is 0 to Vref)
R2	CLOSED	Powers output buffer from +5 V and –5 V supplies. Remove R2 and install it at location R7 to power U1 from 0 V –5 Vdc.

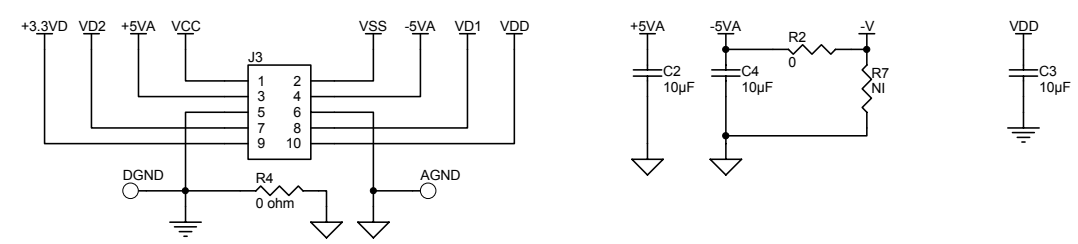
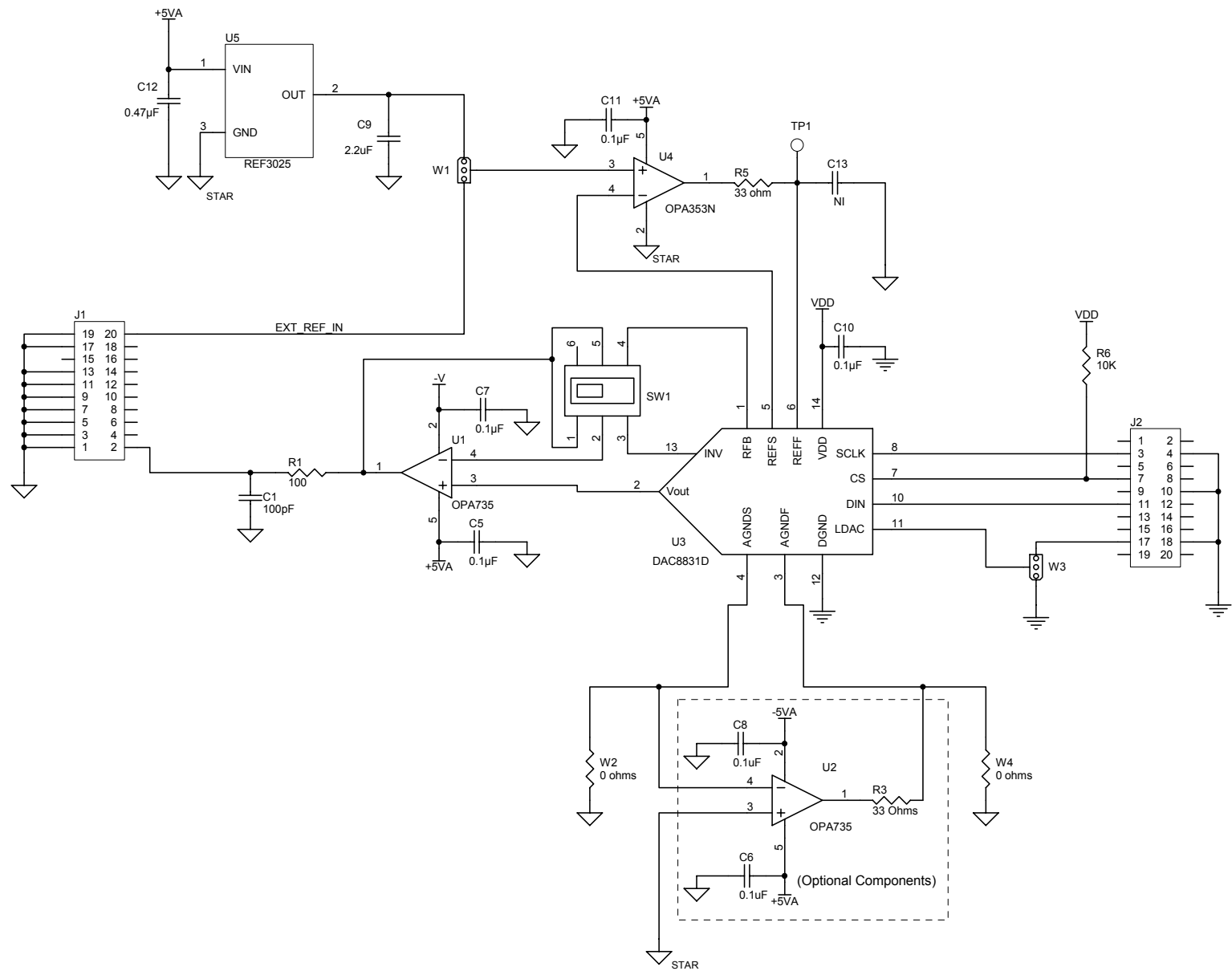
6 EVM BOM and Schematic

Table 5 contains a complete bill of materials for the modular DAC8831 EVM. The schematic diagram is also provided for reference.

Table 5. Bill of Materials

Designators	Description	Manufacturer	Mfg. Part Number
C1	100 pF, 0805, Ceramic, X7R, 25V, 10%	TDK	C0603X5R1E101K
C2 C3 C4	10 μF, 1206, Ceramic, Y5V, 10V, 10%	TDK	C3216Y5V1C106Z
C5 C7 C10 C11	0.1 μF, 0805, Ceramic, X7R, 50V, 10%	TDK	C2012X7R1E104K
C6 C8 C13	Not Installed	TDK	C2012X7R1E104K
C9	2.2 μF, 0805, Ceramic, Y5V, 10V, 10%	TDK	C2012X5R1A225M
C15	0.47 μF, 0805, Ceramic, Y5V, 10V, 10%	TDK	C2012X7R1E474M
J1 J2 (top side)	10 Pin, Dual Row, SMT Header (20 Pos.)	Samtec	TSM-110-01-T-DV-P
J1B J2B(bottom side)	10 Pin, Dual Row, SMT Socket (20 Pos.)	Samtec	SSW-110-22-F-D-VS-K
J3 (top side)	5 Pin, Dual Row, SMT Header (10 Pos.)	Samtec	TSM-105-01-T-DV-P
J3B (bottom side)	5 Pin, Dual Row, SMT socket (10 Pos.)	Samtec	SSW-105-22-F-D-VS-K
R1	100 Ω, 0603, 5%, 0.1 W resistor	Yageo America	9C06031A1000JLHFT
R2 W2 W4	0 Ω, 0805, 5%, 0.1 W resistor	Yageo America	9C06031A0R00JLHFT
R3 R4 R7	Not Installed		
R5	33 Ω, 0603, 5%, 0.1 W resistor	Yageo America	9C06031A33R0JLHFT
R6	10K Ω, 0603, 5%, 0.1 W resistor	Yageo America	9C06031A1002JLHFT
SW1	DPDT Slide Switch	E Switch	EG2209
TP2	Red Test Point Loop	Keystone	5001
DGND AGND	Black Test Point Loop	Keystone	5000
U1	OPA735	TI	OPA735AIDBVT
U2	Not Installed - Optional Component	TI	OPA735AIDBVT
U3	DAC8831	TI	DAC8831IBD
U4	OPA353	TI	OPA353NA
U5	REF3025	TI	REF3025AIDBZT
W1 W3	3 Pin, Single Row, TH Header	Samtec	TSW-103-07-L-S

Revision History		
REV	ECN Number	Approved
A	Initial Release	TH



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 FILE: DAC8831_RA.Sch

DOCUMENT CONTROL # **6470320** REV: **A**

DATE: 21-Jul-2005 SIZE: SHEET: 1 OF: 1

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 0 Vdc to 5 Vdc and the output voltage range of -5 Vdc to 5 Vdc.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 30°C. The EVM is designed to operate properly with certain components above 30°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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